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**OCTOBER 16–17, 2008**
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# PLD Amorphous In-Ga-Zn-O TFTs for Future Optoelectronics

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**Abstract:** *We studied the electrical properties of the room temperature (RT) fabricated amorphous In-Ga-Zn-O thin film transistors (a-IGZO TFTs). The inverted-staggered a-IGZO TFTs fabricated in this work have the following electrical properties: threshold voltage of 4.3V, field-effect mobility of 8.4 $cm^2V^{-1}s^{-1}$, subthreshold swing of 355mV/decade and on/off current ratio over $10^7$. In addition, the a-IGZO thin film shows a very good visible light transparency (closed to 100%). These properties are highly desirable for future optoelectronics.*

**Keywords:** oxide semiconductor, a-IGZO, thin-film transistors (TFTs), active-matrix flat panel displays (AM-FPDs)

## Introduction

Conventional active-matrix (AM) flat panel displays (FPDs) and imagers are based on amorphous or polycrystalline silicon thin film transistor (TFT) technology. Today, hydrogenated amorphous silicon (a-Si:H) thin film can be uniformly deposited on to the glass substrate over large area by plasma enhanced chemical vapor deposition (PECVD) system [1]. Nonetheless, the main limitations of the a-Si:H are electrical instability and a low field-effect mobility ($\mu_{eff}$), which reduces the pixel aperture ratio and driving ability for some demanding applications. Although poly-crystalline silicon TFT has a large field-effect mobility, due to the need of re-crystallization, its electrical properties uniformity over a large area is not always acceptable for a high yield low cost manufacturing and high resolution applications.

Since the next generation flat panel display will require higher resolution, higher brightness and faster operational speed than current standard [2], there is an increasing demand among others for a new semiconductor material to overcome the above mentioned difficulties. Also the future flat-panel photo-imagers [3], will need a larger dynamic range and a smaller pixel size, which cannot be handled by the current a-Si:H TFT backplane technology.

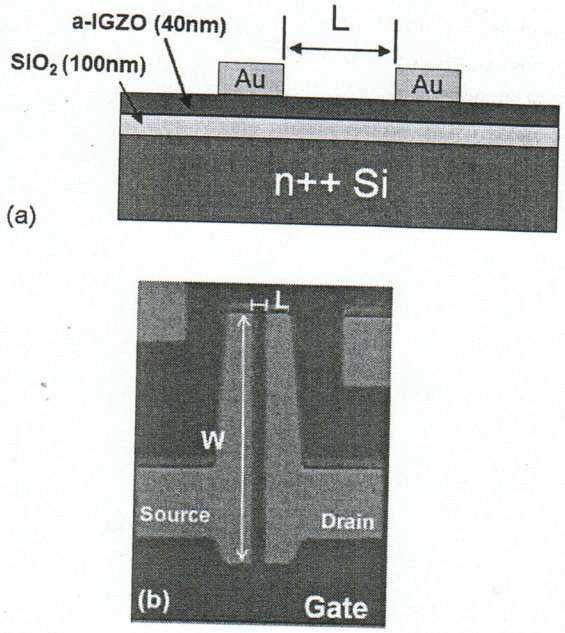


**Figure 1.** (a) Cross-sectional and (b) top view of the inverted-staggered a-IGZO TFT. W and L are TFT channel width and length, respectively.

Since year 2000, there has been a great interest in adapting TFTs made of transparent oxide semiconductors to FPDs. Mono-oxide such as ZnO has been studied extensively but was discovered to have a strong tendency to form polycrystalline phase which is not favorable for making TFT over large area with the uniform electrical properties [4,5]. Recently, multiple-oxides systems drew much more attention due to the improved uniform properties and the ease of forming amorphous phase. Specifically, the ternary oxide system which consists of $In_2O_3$, $Ga_2O_3$ and ZnO has shown promising performance for TFT active layer with high mobility, high resistivity and good uniformity [6]. In this paper, we present the result on amorphous In-Ga-Zn-O (a-IGZO) TFT which is suitable for next-generation AM-FPDs and active-matrix array detectors.

## Experimental

An inverted-staggered a-IGZO TFT structure was used in this study; Figure 1 shows the cross-sectional and top view. We initially selected heavily doped (n++) silicon wafer with 100nm thermal oxide layer as gate electrode and insulator, respectively. A 40nm thick a-IGZO active layer was deposited on the substrate by pulse-laser deposition (PLD) from poly-crystalline $InGaZnO_4$ ceramic target [7]. The deposition was done in an oxygen atmosphere without any intentional substrate heating. Before the source/drain electrodes deposition, a macro-island is formed by edge-dipping/etching in the dilute HCl solution. Finally, a 60nm thick gold (Au) source/drain electrodes were deposited through stencil mask openings by thermal evaporation.

Electrical measurement of the a-IGZO TFT were carried out with a probe station system located in a light tight box. The transistor electrical properties were measured by a PC controlled Agilent 4156 semiconductor parametric analyzer.

## Optical Properties of a-IGZO Thin-Film

The intrinsic optical properties of a-IGZO thin film were investigated. To minimize the background interference, we deposited the a-IGZO thin film directly onto the quartz substrate to measure its optical characteristics. Figure 2 shows the transmission spectrum of a-IGZO thin-film collected by a Cary 5E UV-VIS spectrometer using polarized light [8]. The background contribution from quartz substrate was removed by using the dual beams measurement technique. Very high visible light (λ= 400~

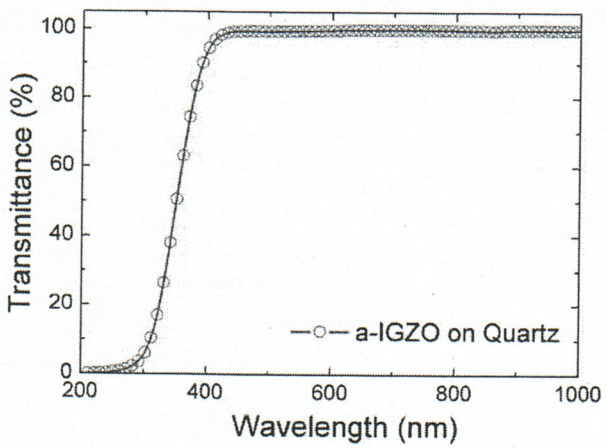


**Figure 2.** Transmission spectrum of the a-IGZO thin film with thickness of 180nm. The background contribution from the quartz substrate was removed by dual beams measurement technique.

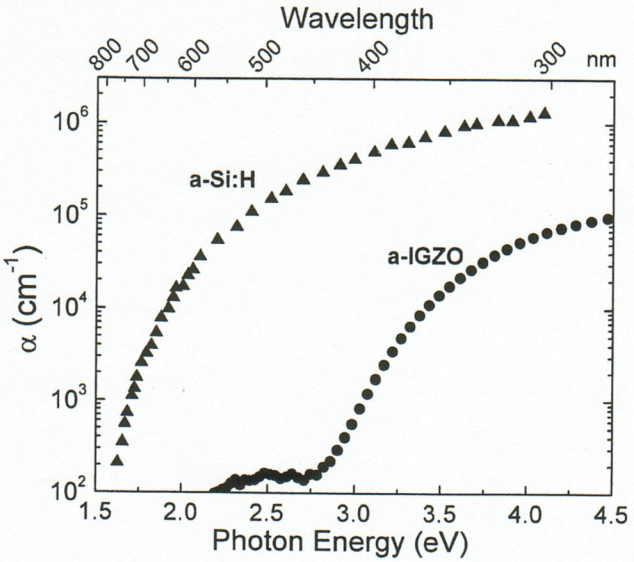


**Figure 3.** Absorption coefficient of a-IGZO (•) and a-Si:H (▲, from [9]) as a function of photo energy and corresponding wavelength.

700nm) transparency is observed with transmittance close to 100%. We further collected the absorption spectrum of a-IGZO sample. Figure 3 shows its absorption coefficient (α) as a function of photon energy (and corresponding wavelength). The α of a-Si:H collected from other group [9] is also shown as a reference. The α of a-IGZO is at least an order of magnitude lower than it's a-Si:H counterpart within the photon energy range we investigated. Take visible light (λ=400~700nm) for example, the α of a-Si:H ranging from 3000 to ~$5\times10^5$ $cm^{-1}$ while α of a-IGZO is well below $10^3 cm^{-1}$ except the near UV region (~400nm). This observation is consistent with the optical gap properties of a-IGZO, which was found to have wide band-gap with Tauc's gap around 3.1eV [10]. Since a-IGZO is essentially "invisible", a-IGZO TFT is suitable for transparent electronics. It also suggests that the aperture ratio of the AM-FPD pixel electrode circuits could be improved by adapting a-IGZO and allowing a direct transmission of the backlight or LED emission through TFTs. For detector, the exceptionally low absorption in visible range is also a potential advantage, which might reduce the need of light shielding in the pixel electrode circuit.

## PLD a-IGZO TFT Electrical Properties

The output characteristics of a-IGZO TFT under various gate voltages ($V_{GS}$) ranging from 4~12V are shown in Figure 4(a). During each measurement, the drain voltage

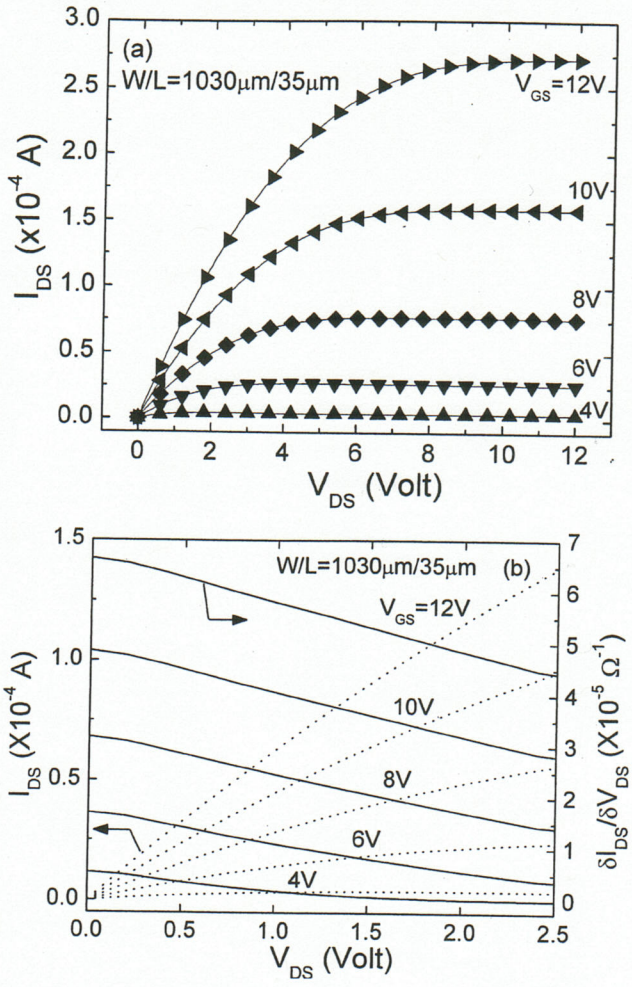


**Figure 4.** (a) Output characteristics of a-IGZO TFT. (b) A zoom-in plot of the output characteristic (dash curves) near the origin ($V_{DS}$=0~2.5V); the derivative of $I_{DS}$ vs $V_{DS}$ characteristics ($\delta I_{DS}/\delta V_{DS}$ , solid curves) are also shown.

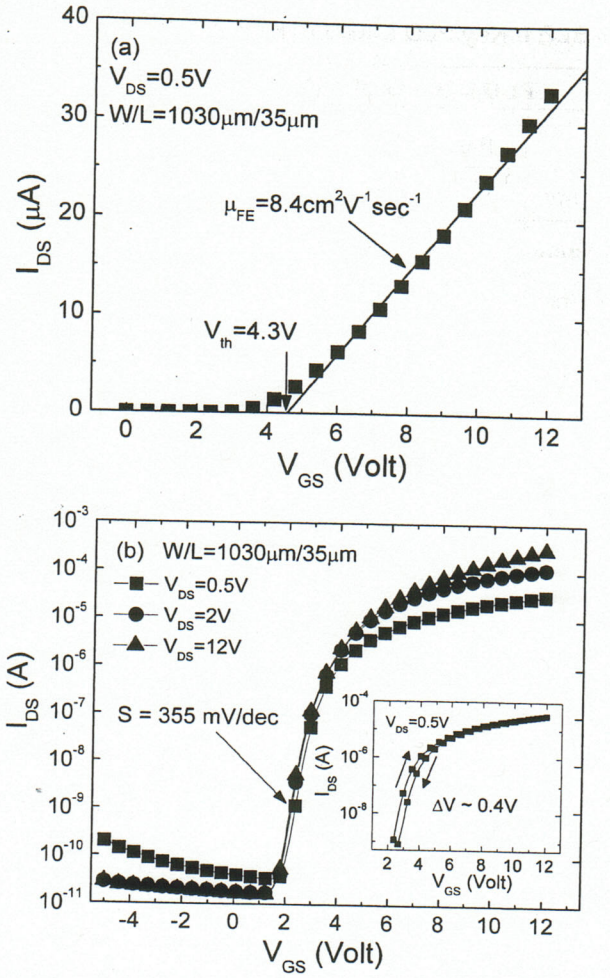


**Figure 5.** (a) Transfer characteristics of a-IGZO TFT in (a) linear plot and (b) semi-log plots. (Inset, b) The TFT hysteresis measured at $V_{DS}$=0.5V; Δ V is the shift in sub-threshold properties.

($V_{DS}$) was varied from 0~12V. A very clear distinction between linear and saturation region is obtained. This suggests that less than 12V of drain voltage ($V_{DS}$) is adequate for operating a-IGZO TFT active-matrix arrays. The TFT source/drain property is another important aspect for TFT evaluation. A non-ohmic source/drain contact, improper active layer thickness (too thick) and high bulk density of states (DOS) can all cause TFT to have a non-linear drain current ($I_{DS}$)/ $V_{DS}$ behavior, also called "current crowding", at low $V_{DS}$ [11,12]. Figure 4(b) shows the output characteristics near the origin ($V_{DS}$=0~2.5V) and there is no current crowding observed in a-IGZO TFT. The absence of current crowding can be better appreciated by plotting the derivative of the output curves ($\delta I_{DS}/\delta V_{DS}$) which is also shown in Figure 4(b). These properties are highly desirable for a-IGZO TFT to be used in active-matrix arrays.

Figure 5(a) illustrates the linear region ($V_{DS}$=0.5V) transfer characteristics of a-IGZO TFT. We extracted the threshold voltage ($V_{th}$) and field effect mobility ($\mu_{eff}$) based on the standard MOSFET equation:

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - V_{th}) V_{DS} \quad (1),$$

where $C_{ox}$ is the gate insulator capacitance per unit area, W and L are TFT channel width and length, respectively. The best linear fit of eq.(1) between 90% to 10% of the maximum $I_{DS}$ (at $V_{GS}$=12V) was found and the $V_{th}$ and $\mu_{eff}$ are determined to be 4.3V and 8.4cm$^2$V$^{-1}$sec$^{-1}$, respectively.

**TABLE I.** Key PLD a-IGZO TFT Electrical Properties

| PLD a-IGZO TFT (W/L=1030μm/35μm) | | | | | |
|---|---|---|---|---|---|
| | $\mu_{eff}$* | $V_{th}$* | S | $I_{DS\_off}$ | On/off current ratio |
| **Unit** | $cm^2/Vs$ | V | mV/decade | A | |
| **Value** | 8.4 | 4.3 | 355 | $\sim 10^{-11}$ | $>10^7$ |

*Extracted by 90%~10% method

The subthreshold swing (S) was also extracted at the maximum slope point ($V_{GS}$=2.37V) from the subthreshold region data (Figure 5(b)), using the following equation:

$$S = \left( \frac{d \log(I_{DS})}{dV_{GS}} \right)^{-1} \quad (2).$$

The S for our a-IGZO TFT is as low as 355mV/dec. Such value is compatible or even superior than a-Si:H TFT. This ensures a fast TFT response and also reduces the voltage of the gate driving signal. Table I summarizes all key TFT properties. We measured the TFT off-state drain current ($I_{DS\_off}$) down to $V_{GS}$= -5V. No significant increase on $I_{DS\_off}$ was observed (The slight increase under $V_{DS}$=0.5V (Fig. 5(b)) was due to the capacitance loading during measurement.) that could be associated with hole-current conduction in TFT channel. Since the devices used in this study have only macro-island patterned, we expected (and was experimentally verified) the $I_{DS\_off}$ (and also the on/off current ratio) to be further improved by incorporating active island in each individual transistor.

## Field-Effect Mobility of PLD a-IGZO TFT

Perhaps the most attracting properties of a-IGZO TFT is its high mobility. Compare to a-Si:H TFT (with $\mu_{eff} \sim 0.5$ $cm^2/Vs$) there is more than an order of magnitude improvement in $\mu_{eff}$ for a-IGZO TFT. In fact the $\mu_{eff}$ extracted by using eq.(1) can be considered as an average value. Further analysis of the linear region transfer data (Figure 5(a)) reveals a non-linear $I_{DS}/V_{GS}$ behavior observed at the higher $V_{GS}$. In other word, the apparent field effect mobility is dependent on $V_{GS}$. This can be better illustrated by defining the incremental field effect mobility ($\mu_{inc}$) with the following relation:

$$\mu_{inc} = \left( \frac{dI_{DS}}{dV_{GS}} \right) \left( \frac{L}{WC_{ox}V_{DS}} \right) \quad (3)$$

and plots it as a function of $V_{GS}$. As shown in Figure 6, $\mu_{inc}$ of the a-IGZO TFT is proportional to the $V_{GS}$ and reaches a

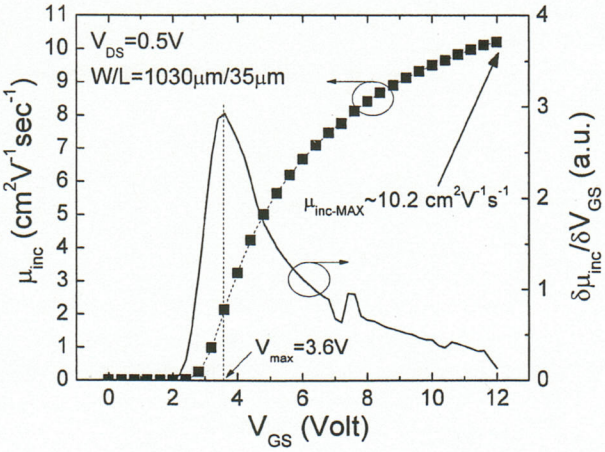


**Figure 6.** The incremental field-effect mobility ($\mu_{inc}$) of the a-IGZO TFT extracted by using eq.(3) (symbol:■). The differentiation of $\mu_{inc}$ ($d\mu_{inc}/dV_{GS}$) is also shown. $V_{max}$ represents the $V_{GS}$ with maximum $d\mu_{inc}/dV_{GS}$.

maximum value of 10.2 $cm^2/Vs$ within our measurement range. Such behavior has also been seen in other oxide semiconductor TFTs [13,14]. It is believed portion of the induced channel charges are trapped in band tail states (or deep states) and cannot contribute to the $I_{DS}$. As $V_{GS}$ increased, more free carriers are able to contribute to the $I_{DS}$ and this makes $\mu_{inc}$ increase toward the intrinsic band mobility. Therefore, to better model the a-IGZO TFT I/V properties, the gate voltage dependent field-effect mobility ($\mu_{eff}(V_{GS})$) is introduced into the standard MOSFET equation (eq.(1)):

$$I_{DS} = \mu_{eff}(V_{GS}) C_{ox} \frac{W}{L} (V_{GS} - V_{th}) V_{DS} \quad (4)$$

and $\mu_{eff}(V_{GS})$ can be described as:

$$\mu_{eff}(V_{GS}) = \mu_0 \left( \frac{V_{GS} - V_{th}}{V_C} \right)^{\alpha} \quad (5)$$

where $\mu_0$ is the intrinsic band mobility, $V_c$ is the material dependent critical voltage and $\alpha$ is the power coefficient which describes the dependence of $\mu_{eff}(V_{GS})$ on effective gate voltage ($V_{GS}$-$V_{th}$). As a comparison, in ideal case, $\alpha$=0 and $\mu_{eff}(V_{GS}) = \mu_{eff} = \mu_0$. For the ease of parameter extraction, eq.(5) is further simplified as:

$$\mu_{eff}(V_{GS}) = K(V_{GS} - V_{th})^{\alpha} \quad (6)$$

where K is the material dependent fitting parameter. It should be noticed that the K has the unit of $cm^2/V^{\alpha+1}s$. By substituting eq.(6) into eq.(4), new $I_{DS}$ equation can be

written as:

$$I_{DS} = KC_{ox}\frac{W}{L}(V_{GS}-V_{th})^{\alpha+1}V_{DS} \quad (7)$$

$$= KC_{ox}\frac{W}{L}(V_{GS}-V_{th})^{\gamma}V_{DS} \quad (8)$$

where

$$\gamma \equiv \alpha + 1 \quad (9).$$

From eq.(6) and eq.(9), we can derive:

$$\mu_{eff}(V_{GS}) = K(V_{GS}-V_{th})^{\gamma-1} \quad (10),$$

and from eq.(3) and eq.(8), incremental field effect mobility can be describe as:

$$\mu_{inc} = K\gamma(V_{GS}-V_{th})^{\gamma-1} \quad (11).$$

Special care should be made to properly extract the $V_{th}$, $\gamma$ and K. Directly perform a non-linear fitting of the entire transfer data to eq.(8) is not an ideal approach because this can introduce unwanted subthreshold region data into the fitting algorithm which causes error. In this study, we propose two different methodologies which are suitable for device parameter extraction. The first method (method #1) is adapted from what was developed for a-Si:H TFT [15]. The determination of threshold voltage is based on eq.(8). By varying $V_{th}$, we find the least-square linear fit to the logarithm of drain current ratio:

$$\log\left(\frac{I_{DS}}{I_0}\right) = \gamma\log\left(\frac{V_{GS}-V_{th}}{V_0-V_{th}}\right) \quad (12)$$

where the reference drain current, $I_0=I_{DS}(V_{GS}=V_0)$, and is chosen to be much larger than the subthreshold current. In this study, $V_0$=6V with $I_0$= 6.32μA were chosen. Figure 7 shows the RMS error and corresponding $\gamma$ of the linear fit to eq.(12) as a function of $V_{th}$. The $V_{th}$ and $\gamma$ are determined simultaneously by the best linear fit with minimum error. As indicated in Figure 7, $V_{th}$ and $\gamma$ are 3.5V and 1.36, respectively. K (=3.57) is finally extracted by performing a best non-linear fit of above threshold transfer data to eq.(8).

Although the first method (method #1) can accurately extract $V_{th}$ and $\gamma$ simultaneously, the procedure is rather complicated and not straight forward. Our second approaches (method #2) extract $V_{th}$, $\gamma$ and K separately in a two steps process. A similar method has also been used to extract the threshold voltage of the a-Si:H TFT [1]. The $V_{th}$ is first defined as the $V_{GS}$ value at which maximum $d\mu_{inc}/dV_{GS}$ occurs ($V_{max}=V_{th}$=3.6V, as illustrated in

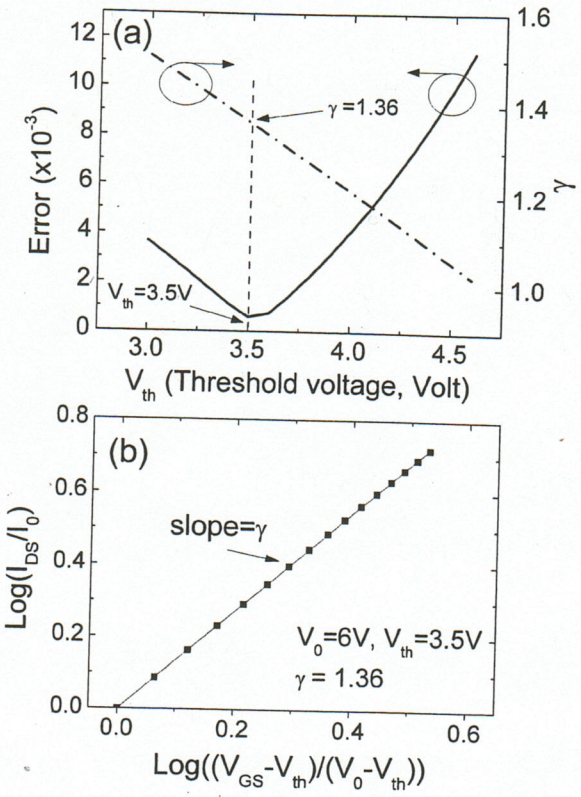


**Figure 7.** (a) Variation in $\gamma$ of the experimental I-V data in above threshold region as a function of $V_{th}$. A reference gate voltage $V_0$ of 6V is used for parameter extraction. Also shown is the RMS error of the least-square linear fit to the log of drain current ratio ($Log(I_{DS}/I_0)$). (b) Example of actual linear fitting plot to eq.(12) at $V_{th}$ with minimum error (3.5V).

Figure 6). The "change" of $\mu_{inc}$ v.s. $V_{GS}$ has two opposite behaviors between sub- and above threshold regions: in subthreshold region, $\mu_{inc}$ increases exponentially with $V_{GS}$ and the $d\mu_{inc}/dV_{GS}$ is increasing with $V_{GS}$. However, in above threshold region, $d\mu_{inc}/dV_{GS}$ is decreasing with $V_{GS}$, and $\mu_{inc}$ will eventually saturate at certain value (eg. intrinsic band mobility, $\mu_0$). Consequently, the maximum $d\mu_{inc}/dV_{GS}$ point represents the transition between these two regions, where $V_{th}$ located. The authors believe such phenomenon is fundamentally due to the difference in a-IGZO deep gap and band tail density-of-states (DOS) properties. The $\gamma$-1 (or $\alpha$) and K is then extracted from the linear fit of the log-log plot of eq.(11):

$$\log(\mu_{inc}) = \log(K\gamma) + (\gamma-1)\log(V_{GS}-V_{th}) \quad (13)$$

, as shown in Figure 8. In summary, the $V_{th}$, $\gamma$ and K extracted by method #2 are 3.6V, 1.37 and 3.47, respectively. Figure 9 shows the results obtained from

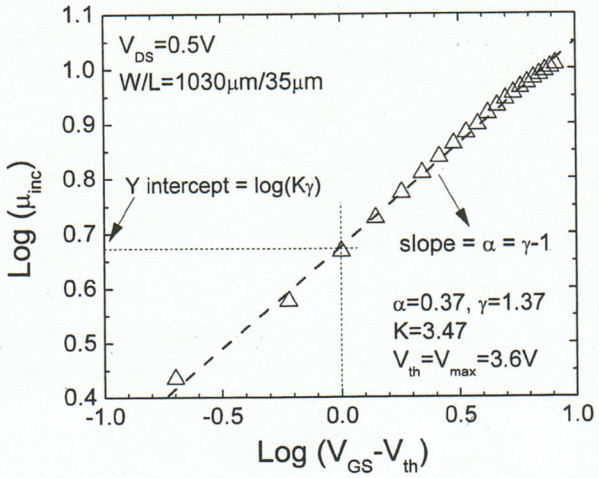


**Figure 8.** The log-log plot of the incremental field-effect mobility ($\mu_{inc}$) as a function of the effective gate voltage ($V_{GS}$-$V_{th}$). The $V_{th}$ is extracted from $V_{max}$ in Figure 6. Dash line is the linear fit to the experimental data (symbol: △ ).

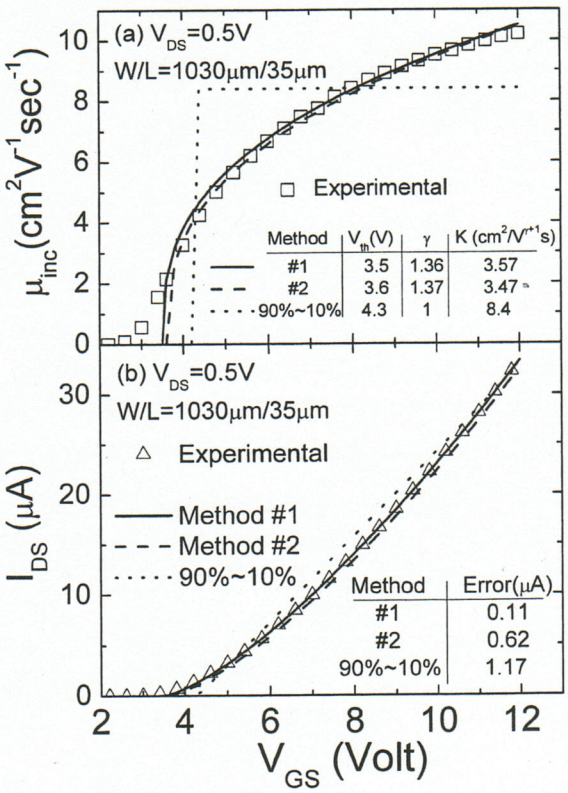


**Figure 9.** The calculation of (a) $\mu_{inc}$ and (b) $I_{DS}$ based on different models/extraction methods used in this study. Method #1 is conducted in Figure 7. Method #2 is illustrated in Figure 8. The 90%~10% method is conducted based on the standard MOSFET equation (eq.(1)). Symbols: experimental data.

various models/methodologies discussed in this study. The table in Figure 9(a) summarized the extracted parameters by using different methods. The $\mu_{inc}$ and $I_{DS}$ are calculated by substituting corresponding parameters into eq.(11) and eq.(8), respectively. Results obtained from method #1 and #2 are consistent with each other and they are fairly closed to the experimental data. RMS errors for $I_{DS}$ calculated by different methods are also provided in Figure 9(b) and method #1 has the lowest error. It is clear that the eq.(6) is suitable for describing gate voltage dependent field-effect mobility, $\mu_{eff}(V_{GS})$, which is essential to accurately model the a-IGZO TFT I/V properties.

## TLM Analysis of PLD a-IGZO TFT

The contact resistance was extracted by transmission line method (TLM) [16]. Only a constant, $V_{GS}$ independent field-effect mobility ($\mu_{TLM}$) is considered and the total TFT on resistance can be written as:

$$R_T = \frac{V_{DS}}{I_{DS}} = 2R_0 + \frac{L + 2\Delta L}{\mu_{TLM} C_{ox} W (V_{GS} - V_{th\_TLM})} \qquad (14)$$

and

$$r_{ch} = 1/(\mu_{TLM} C_{ox} W (V_{GS} - V_{th\_TLM})) \qquad (15).$$

where $R_0$ is the S/D contact resistance and Δ L is the channel length bias. As illustrated in Figure 10, the total TFT on-resistance ($R_T$) has been plotted as a function of TFT channel length for different gate voltage ($V_{GS}$=9~12V). $R_0$ and Δ L can be extracted from the cross-point and they are 3.3kΩ and -11.3μm, respectively. For even lower $V_{GS}$,

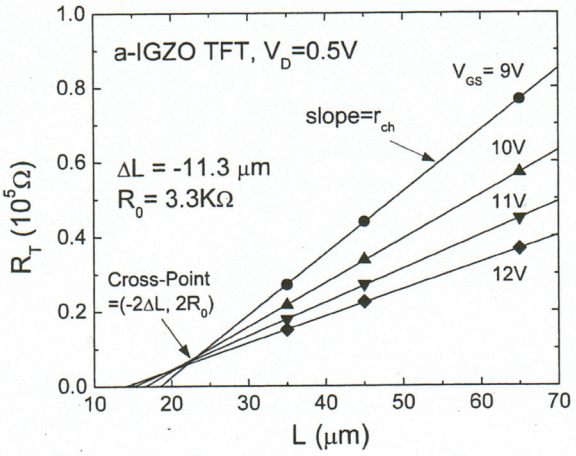


**Figure 10.** Illustration of the TLM used to extract S/D contact resistances and TFT properties. Symbol: experimental data, solid lines: linear fit.

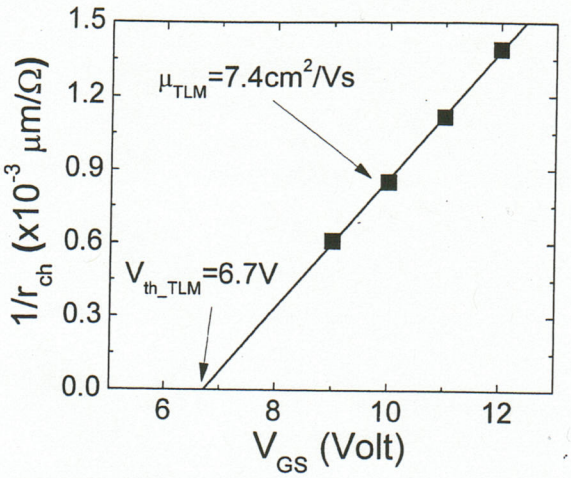


**Figure 11.** The evolution of $1/r_{ch}$ extracted from TLM analysis with TFT gate voltage. Symbol: experimental data, solid lines: linear fit.

due to additional $V_{GS}$ dependence of $R_0$ and $\Delta L$, we observed a shift on the cross-point. The low $R_0$ indicates the S/D metal (Au) is forming an ohmic like contact with a-IGZO. In comparison, $R_0$ of a-Si:H TFT is usually on the order of $10^5$~$10^6\Omega$. We believe that the negative $\Delta L$ is due to a metal diffusion from S/D into the channel region which causes the effective gate length to be shorter than the designed value. We also extract the field effect mobility ($\mu_{TLM}$=7.4cm²/Vs)) and threshold voltage ($V_{th\_TLM}$=6.7V) from TLM data (Figure. 11). The discrepancy between results extracted by TLM and 90%~10% method can be explained by the following: (1) the shorter effective gate length could cause an overestimation of the mobility in standard 90%~10% method, which doesn't consider $\Delta L$; if $\Delta L$ is consider, the $\mu_{eff}$ extracted by 90%~10% will be ~3cm²/Vs; (2) TLM is only effective in high $V_{GS}$ region (9~12V) which cause an overestimation in threshold voltage ($V_{th\_TLM}$); (3) more experimental points are needed to fit better this data. The TLM analysis suggests the S/D metal and contact interface should be improved to suppress the metal diffusion and enhance the linearity of the channel length dependence on a-IGZO TFT properties. Finally, the current TLM method doesn't consider the dependence on $V_{GS}$ for field effect mobility. By introducing the $\gamma$ into eq.(14) and (15), the non-linear evolution of $1/r_{ch}$ vs. $V_{GS}$ can be modeled and the intrinsic TFT properties can be better extracted.

## Conclusion

We have successfully fabricated the inverted stagger a-IGZO TFT by pulse-laser deposition (PLD). All processing steps are performed at room temperature without any additional thermal treatment. This process is highly desirable for device fabrication over large area or flexible substrate where a low thermal-budget process is necessary. Compare to a-Si:H TFT, a-IGZO TFT have more than ten times higher field-effect mobility and an excellent switching properties. These make a-IGZO TFT very suitable candidate for pixel electrode circuits for future AM- LCDs or AM-OLEDs requiring a high resolution, fast response and high brightness. In addition, a-IGZO TFT can be used in active-pixel back plane for detectors. A high mobility can enhance the pixel signal gain and allow the designer to achieve a higher dynamic range without sacrificing pixel size. Finally, a-IGZO was found to have a very high visible light transparency which makes it very attractive for future transparent electronics.

## Acknowledgement

The authors (T.-C. Fung and J. Kanicki) would like to thank DARPA HARDI program for their financial support.

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